T Tushar Shenoy

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CAREER OBJECTIVE

Aspiring Electronics and Communication engineer with a strong focus on VLSI and Embedded Systems, seeking an opportunity to leverage my knowledge and hands-on experience. With a proactive mindset, rapid learning ability and a commitment to continuous development, I aim to contribute effectively to my team and drive impactful results for my organization.

Aspiring Electronics and Communication Engineer with a strong focus on VLSI and RTL design. Seeking opportunities to leverage my hands-on experience and technical knowledge in digital design. I bring a proactive mindset, strong learning agility and a commitment to continuous improvement, aiming to contribute effectively and deliver impactful results.

EDUCATION

N.M.A.M. Institute of Technology, Nitte | 2021 – 2025
B.E. Electronics and Communication | Grade: 9.42/10

Canara Pre-University college, Mangaluru | 2019 – 2021
PU PCME | Grade: 99.16%

Kendriya Vidyalaya No. 1, Panambur | 2019
CBSE | Grade: 91.6%

PROFESSIONAL EXPERIENCE

Hardware Design Engineer | Anmaya Technologies
10/2025-present
- Working on RTL design and FPGA implementation for communication and satellite systems, including signal processing and RF-interfaced architectures.
- Handling full FPGA development flow from RTL to Hardware Validation
- Debugging complex designs using Vivado ILA/VIO and performing board bring-up on custom hardware platforms.
- Leading intern mentorship and conducting technical workshops on FPGA and embedded systems.

RTL Design Intern | Samsung Semiconductor India Research
01/2025 - 07/2025
- Cache Controller IP Development – Designed and implemented a 64KB, 4-way set-associative cache controller with write-back and write-allocate policies.
- Developed microarchitecture with tag, data, LRU and write-back blocks, including memory banking for improved data throughput.
- Implemented cache flush and invalidation mechanisms. Resolved synthesis and lint violations and verified the design with extensive test cases, including hit/miss scenarios, back-to-back operations and dirty block handling.

SKILLS

Hardware Description Languages — Verilog, SystemVerilog (Familiar with syntax and testbench creation)

Cadence EDA Tools — Virtuoso, Xcelium, Innovus

FPGA Tools — Xilinx ISE, Vivado, Intel Quartus Prime

Programming languages: — C, Python

CERTIFICATIONS

Verilog Language and Application v27.0 Exam
Cadence | 01/2025

CMOS Digital VLSI Design
NPTEL | 01/2024 - 03/2024

Embedded System Design with ARM
NPTEL | 01/2024 - 03/2024

Microelectronics: Devices to Circuits
NPTEL | 07/2023 - 10/2023

PUBLICATIONS & PROJECTS

PUBLICATION : Smart Insole Design for Foot Pressure Monitoring
VSPICE-2023, Springer | 19/12/2023 - 20/12/2023
- Presented and published the research paper in a Springer journal at the VSPICE-2023 conference held on 19th & 20th December 2023 at NMAMIT, Nitte

IoT-Enabled Payment Gateway for Product Dispensing or Action After Payment
NMAM Institute of Technology | 7/2024 - 11/2024
- Developed an IoT-enabled payment gateway using ESP32, integrating UPI transactions with real-time tracking via Google Firebase. Designed a custom vending machine with a TFT display, dynamic QR code generation and secure, cashless payments through Razorpay, eliminating physical currency.

Study Of ADS1293 – Three Channel Biopotential For ECG
NMAM Institute of Technology | 02/2024 - 05/2024
- Developed an ECG monitoring system using the ADS1293 analog front-end (AFE) interfaced with NI myRIO via high-speed SPI communication.

4-Bit Johnson Counter
NMAM Institute of Technology | 07/2023 - 08/2023
- Developed a 4-bit Johnson counter in Verilog using D flip-flops with asynchronous reset. Created an OOP-based test bench and package to verify the counter's functionality and compare its output to the expected sequence.

4-BIT Binary Code Converter
NMAM Institute of Technology | 12/2022 - 02/2023
- Designed a 4-bit binary code converter using multiplexers, demultiplexers and logic gates to convert binary codes into Gray code, BCD and Excess-3 formats.

ACTIVITIES & WORKSHOPS

Resource Person – Proteus Workshop
NMAMIT | 05/10/2024

Resource Person – ESP-IDF Workshop
NMAMIT | 28/09/2024

Participant – Semi-Custom and Full Custom VLSI Design using Cadence
NMAMIT | 17/01/2024 - 18/01/2024

Participant – Nitte Healthcare Innovation Hackathon 2023
NMAMIT | 05/05/2023 - 07/05/2023

Participant – Digital Design using Intel FPGAs
MSIS | 02/03/2023 - 03/03/2023